Xin "Felicity" Fu, Ph.D.

Assistant Professor
Department of Electrical and Computer Engineering
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Research Interests

Computer Engineering; Computer architecture; Energy-efficient computing; High-performance computing; Hardware reliability and variability; Mobile computing; Heterogeneous computing; Emerging technologies (e.g. non-volatile memory, near-threshold computing, 3D integration); General-purpose computing on graphics processing units (GPGPUs); Dark silicon; On-chip interconnection network;

Education

- **NSF Computing Innovation Fellow,** Computer Science Department, University of Illinois at Urbana-Champaign, September 2009 ~ July 2010
  Advisor: Dr. Sarita Adve

- **Ph.D.** in Computer Engineering, University of Florida, USA, December 2009
  Dissertation: Characterizing, Modeling and Mitigating Microarchitecture Vulnerability and Variability in Light of Small-Scale Processing Technology
  Advisor: Dr. Tao Li and Dr. Jose Fortes

- **Graduate Studies** in Computer Software and Theory, Central South University, China, August 2003 ~ August 2004
  Advisor: Dr. Songqiao Chen

- **B.E.** in Computer Science and Technology, Central South University, China, July 2003
  Thesis: Design and Implementation of Fingerprint Model Training System for Web Site
  Advisor: Dr. Songqiao Chen and Dr. Hongfei Sui

Working Experiences

- **Assistant Professor,** Electrical and Computer Engineering Department, University of Houston, September 2014 ~ present

- **Assistant Professor,** Electrical Engineering and Computer Science Department, University of Kansas, August 2010 ~ August 2014

- **NSF Computing Innovation Fellow,** Computer Science Department, University of Illinois at Urbana-Champaign, September 2009 ~ July 2010

- **Research Assistant,** Electrical and Computer Engineering Department, University of Florida, August 2004 ~ August 2009

- **Research Assistant,** School of Information Science and Engineering, Central South University, China January 2003 ~ August 2004

Research Grants

- **National Science Foundation**, **CAREER: New Foundations for Next-Generation Reliable Throughput Architecture Design**, Xin Fu (single PI), $430,000, 5/15/2014 ~ 5/14/2019

- **National Science Foundation**, **SHF: Small: Collaborative Research: Exploring Energy-Efficient GPGPUs through Emerging Technology Integration**, Xin Fu (PI), $239,672, 8/1/2013 ~ 7/31/2016

- **National Science Foundation**, Maximizing the Utilization of Renewable Energy to Optimize the Soft-Error Robustness of GPGPU-based Data Centers, Xin Fu (single PI), $136,939, 5/1/2012 ~ 9/30/2013

- **National Science Foundation**, Student Travel Support for the Twenty-First International Conference on Parallel Architectures and Compilation Techniques, Xin Fu (single PI), $12,000, 8/15/2012 ~ 7/31/2013

- **University of Kansas,** GRF: Bridging the Gap between Processor Optimization Approaches and Design Goals via Predictive Models, Xin Fu (single PI), $8,062, 7/1/2014~6/30/2015

- **University of Kansas**, GPGPU-SODA: A Unified Framework for GPGPU Soft-Error Dependability Analysis, Xin Fu (single PI), $8,000, 5/20/2012~6/20/2012

- **National Science Foundation and Computing Research Association**, Gate-level Fault Injection and Tolerance on Multi-core FPGA-based System, Xin Fu (single PI), $280,000, 9/30/2009 ~ 9/29/2011

Publications

[1] Jingweijia Tan, and Xin Fu, Mitigating the Susceptibility of GPGPUs Register File to Process Variations, International Parallel & Distributed Processing Symposium (**IPDPS**), 2015 **(Acceptance rate: 21.8%)**

[2] Kaige Yan, and Xin Fu, Energy-Efficient Cache Design in Emerging Mobile Platforms: The Implications and Optimizations, Design, Automation, and Test in Europe (**DATE**), 2015 **(Acceptance rate: 22.4%)**

[3] Jingweijia Tan, Zhi Li, and Xin Fu, Soft-Error Reliability and Power Co-Optimization for GPGPUs Register File using Resistive Memory, Design, Automation, and Test in Europe (**DATE**), 2015 **(Acceptance rate: 22.4%)**

[4] Mingsong Chen, Daian Yue, Xiaoke Qin, Xin Fu and Prabhat Mishra, Variation-Aware Evaluation of MPSoC Task Allocation and Scheduling Strategies using Statistical Model Checking, Design, Automation, and Test in Europe (**DATE**), 2015 **(Acceptance rate: 22.4%)**

[5] Zhongqi Li, Amer Qouneh, Madhura Joshi, Wangyuan Zhang, Xin Fu, and Tao Li, Aurora: A Cross-Layer Solution for Thermally Resilient Photonic Network-on-Chip, in IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**), Volume PP, Issue 99, February 2014

[6] Ying Zhang, Lide Duan, Bin Li, Lu Peng, and Xin Fu, Design Configuration Selection for Hard-error Reliable Processors via Statistical Rules, in Elsevier Journal of Microprocessors and Microsystems (**MICPRO**), Volume 38, Issue 1, February, 2014

[7] Jingweijia Tan, Yang Yi, Fangyang Shen, and Xin Fu, Modeling and Characterizing GPGPU Reliability in the Presence of Soft Errors, In Elsevier Journal of Parallel Computing, Volume 39, Issue 9, September 2013

[8] Ying Zhang, Lu Peng, Xin Fu, and Yue Hu, Lighting the Dark Silicon on Future Processors: A Comprehensive Evaluation of New Design Dimensions, Design Automation Conference **(DAC)**, June 2013 **(Acceptance rate: 21%)**

[9] Yang Yi, Yaping Zhou, and Xin Fu, Modeling Differential Through-Silicon-Vias (TSVs) with Voltage Dependent and Nonlinear Capacitance, in Journal of Selected Areas in Microelectronics (**JSAM)**, June Edition, Volume 3, Issue 6, 2013

[10] Jingweijia Tan, Zhi Li, and Xin Fu, Cost-Effective Soft-Error Protection for SRAM-Based Structures in GPGPUs, International Conference on Computing Frontiers **(CF)**, May 2013

[11] Zhi Li, Jingweijia Tan, and Xin Fu, Hybrid CMOS-TFET Register Files for Energy-Efficient GPGPUs, International Symposium on Quality Electronic Design **(ISQED)**, March 2013

[12] Xin Fu, Tao Li, and José Fortes, Reliable Express Virtual Channel Based Network-on-Chip Under the Impact of Technology Scaling, International Symposium on Quality Electronic Design **(ISQED)**, March 2013

[13] Jingling Yuan, Xin Fu, and Tao Li, Intelligent Spatial-based Resource Allocation Algorithms in NoC, in Special Issue on Parallel Computing, Journal of Computers, Volume 8, Issue 3, March 2013

[14] Amer Qouneh, Zhongqi Li, Madhura Joshi, Wangyuan Zhang, Xin Fu, and Tao Li, Aurora: A Thermally Resilient Photonic Network-on-Chip Architecture, International Conference on Computer Design **(ICCD)**, Montreal, Quebec, Canada, October 2012 **(Acceptance rate: 26%)**

[15] Jingweijia Tan, and Xin Fu, RISE: Improving Streaming Processors Reliability against Soft Errors in GPGPUs, International Conference on Parallel Architectures and Compilation Techniques **(PACT)**, Minneapolis, Minnesota, USA, September 2012 **(Acceptance rate: 18%)**

[16] Andrea Pellegrini, Rob Smolinski, Lei Chen, Xin Fu, Siva Kumar Sastry Hari, Junhao Jing, Sarita Adve, Todd Austin, and Valeria Bertacco, CrashTest'ing SWAT: Accurate, Gate-Level Evaluation of Symptom-Based Resiliency Solutions, Design Automation & Test in Europe **(DATE)**, March 2012 **(Acceptance rate: 27%)**

[17] Jingweijia Tan, Nilanjan Goswami, Tao Li, and Xin Fu, Analyzing Soft-Error Vulnerability on GPGPU Microarchitecture, In Proceedings of IEEE International Symposium on Workload Characterization **(IISWC)**, November 2011

[18] Andrea Pellegrini, Rob Smolinski, Lei Chen, Xin Fu, Siva Kumar Sastry Hari, Junhao Jing, Sarita Adve, Todd Austin, and Valeria Bertacco, CrashTest'ing SWAT: Accurate, Gate-Level Evaluation of Symptom-Based Resiliency Solutions, in Seventh Workshop on Silicon Errors in Logic - System Effects **(SELSE 7)**, March 2011

[19] Xin Fu, Tao Li, and José Fortes, Architecting Reliable Multi-core Network-on-Chip for Small-Scale Processing Technology, International Conference on Dependable Systems and Networks **(DSN)**, June 2010 **(Acceptance rate: 23%)**

[20] Xin Fu, Tao Li, and José Fortes, Soft Error Vulnerability Aware Process Variation Mitigation, International Symposium on High-Performance Computer Architecture **(HPCA)**, February 2009 **(Acceptance rate: 19%)**

[21] Xin Fu, Tao Li, and José Fortes, NBTI Tolerant Microarchitecture Design in the Presence of Process Variation, International Symposium on Microarchitecture **(MICRO)**, November 2008 **(Acceptance rate: 19%)**

[22] Xin Fu, Tao Li and José Fortes, ORBIT: Effective Instruction Queue Soft-error Vulnerability Mitigation on Simultaneous Multithreaded Architectures using Operand Readiness-based Instruction Dispatch, International Symposium on Computer Architecture and High Performance Computing **(SBAC-PAD)**, October 2008

[23] Xin Fu, Wangyuan Zhang, Tao Li and José Fortes, Optimizing Issue Queue Reliability to Soft Error on Simultaneous Multithreaded Architectures, International Conference on Parallel Processing **(ICPP)**, September 2008

[24] Xin Fu, Tao Li and José Fortes, Combined Circuit and Microarchitecture Techniques for Effective Soft Error Robustness in SMT Processors, International Conference on Dependable Systems and Networks **(DSN)**, June 2008 **(Acceptance rate: 23%)**

[25] Xin Fu, Wangyuan Zhang, Tao Li and José Fortes, Optimizing Issue Queue Reliability to Soft Error on Simultaneous Multithreaded Architectures, Workshop on Unique Chips and Systems **(UCAS)** (Held in conjunction with International Symposium on Performance Analysis of Systems and Software), April 2008

[26] Wangyuan Zhang, Xin Fu, Tao Li and José Fortes, An Analysis of Microarchitecture Vulnerability to Soft Errors on Simultaneous Multithreaded Architectures, International Symposium on Performance Analysis of Systems and Software **(ISPASS)**, April 2007

[27] Xin Fu, James Poe, Tao Li and José Fortes, Characterizing Microarchitecture Soft Error Vulnerability Phase Behavior, International Symposium on Modeling, Analysis, and Simulation of Computer and Telecommunication Systems **(MASCOTS)**, September 2006 **(nominated for best paper award)**

[28] Xin Fu, Tao Li and José Fortes, Sim-SODA: A Unified Framework for Architectural Level Software Reliability Analysis, Workshop on Modeling, Benchmarking and Simulation **(MOBS)** (Held in conjunction with International Symposium on Computer Architecture), June 2006

[29] Hongfei Sui, Songqiao Chen, Jianer Chen and Xin Fu, Design and Implementation of Fingerprint Model Training System for Web Site, In Journal of Computer Engineering and Applications, Vol.40 No.12 2004

Teaching Experiences

- ECE7373 Advanced Topics in Computer Architecture (Spring 2015)
- ECE4436 Microprocessor Systems (Fall 2014)
- EECS443 Digital Systems Design (Spring 2014, Spring 2013)
- EECS743 Advanced Computer Architecture (Spring 2014, Spring 2013, Spring 2012, Fall 2010)
- EECS643 Advanced Computer Organization (Fall 2013, Fall 2012, Fall 2011)
- EECS645 Computer Architecture (Spring 2011)

Students

- **Current advisees**

  Jingweijia Tan, Ph.D. student, estimated to complete in Summer 2016

  Kaige Yan, Ph.D. student, estimated to complete in Summer 2016

  Xingyao Zhang, Ph.D. student, estimated to complete in Summer 2019

  Tong Yang, M.S. student, estimated to complete in Summer 2016

- **Alumni**

  Zhi Li, MS, completed in May 2013

  Thesis: Power Modeling and Optimizations for GPGPUs

- **Collaborators**

  Ying Zhang, Ph.D., completed in December 2013, advised by Prof. Lu Peng

  Marianne Jantz, MS, completed in May 2013, advised by Prof. Prasad Kulkarni

  Zhongqi Li, Ph.D., completed in December 2012, advised by Prof. Tao Li

  Madhura R Joshi, MS, completed in December 2011, advised by Prof. Tao Li

  Pradeep Purushothaman, MS, completed in December 2008, advised by Prof. Tao Li

- **Ph.D. and Master Committee**

  Jingweijia Tan, Ph.D. student (Chair), estimated to complete in Summer 2016

Kaige Yan, Ph.D. student (Chair), estimated to complete in Summer 2016
Xingyao Zhang, Ph.D. student (Chair), estimated to complete in Summer 2019
Tong Yang, M.S. student (Chair), estimated to complete in Summer 2016
Zhi Li, MS (Chair), completed in May 2013
Abdulmalik Abdullah Humayed, Ph.D. student, estimated to complete in Summer 2017
Michael Jantz, Ph.D. student, completed in Summer 2014
Wesley Peck, Ph.D., completed in December 2011
Joseph D St Amand, MS student, completed in Summer 2014
Goutham Selvakumar, MS, completed in June 2013
Marianne Jantz, MS, completed in May 2013
Ranjith Pazhangeril Krishnan, MS, completed in May 2013
Hemaiyer Sankaranarayanan, MS, completed in March 2012

Awards and Honors

- **NSF CAREER Award,** 2014
- Miller Scholar, University of Kansas, 2014
- Kansas **NSF EPSCoR First Award**, 2012
- ISCA Travel Grant, ISCA, 2011
- National Science Foundation **Computing Innovation Fellow (CIFellow)** , 2009
- HPCA Student Travel Grant, HPCA, 2009
- MICRO Student Travel Grant, MICRO, 2008
- DSN Student Travel Grant, DSN, 2008
- ISCA Student Travel Grant, ISCA, 2006
- Privilege to enter Graduate School exempted from Entrance Exam, Central South University, 2003
- Outstanding Graduate Student, Central South University, China, 2003
- Excellent Undergraduate Thesis, Central South University, China, 2003
- Xi Nan Lv Fellowship, Xi Nan Lv Company, China, 2002
- Hai Nan Airline Fellowship, Hai Nan Airline, China, 2001
- Champion of English Drama Competition, Central South University, 2001
- Outstanding Undergraduate Student, Central South University, China, 2000 ~ 2001
- Outstanding Undergraduate Student, Central South University, China, 1999 ~ 2000
- Central South University First-class (top 2%) Scholarship, Central South University, 8 times during 1999 ~ 2003

Professional Activities

- **Conference Organization**

2015 Great Lakes Symposium on VLSI, publicity chair
2014 International Symposium on Workload Characterization (IISWC), registration chair
2014 International Symposium on High-Performance Computer Architecture (HPCA), financial chair
2013 International Conference on Networking, Architecture, and Storage (NAS), submission chair
2013 International Symposium on High-Performance Computer Architecture (HPCA), student travel grant chair

2012 International Conference on Parallel Architecture and Compilation Techniques (PACT), student travel grant chair

2012 International Symposium on Computer Architecture (ISCA), web chair

- **Conference Session Chair**

2012 International Conference on Parallel Architecture and Compilation Techniques (PACT)
2013 Missouri, Iowa, Nebraska, Kansas Women in Computing (MINK WIC)

- **Technical Program Committee**

2015, 2013 International Workshop on the Interaction amongst Virtualization, Operating Systems and Computer Architecture (WIVOSCA)

2014 International Workshop on Dependable GPU Computing

2014 International Conference on Computing Frontiers (CF)

2014, 2013 International Parallel & Distributed Processing Symposium (IPDPS)

2014 International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), external review committee

2013 International Workshop on General Purpose Processing on Graphics Processing Units (GPGPU-6)

2012 International Workshop on Unique Chips and Systems (UCAS)

2012 International Workshop on Power-Aware Systems and Architectures (PASA)

- **Reviewer for the international conferences and journals**

IEEE Computer Architecture Letters (CAL), 2015, 2012

IEEE International Symposium on High-Performance Computer Architecture (HPCA), 2015, 2013, 2012, 2011

ACM Transactions on Design Automation of Electronic Systems (TODAES), 2015, 2013

Microelectronics Journal, 2015

ACM Transactions on Architecture and Code Optimization (TACO), 2015, 2013, 2012

IEEE Transaction on Computers (TC), 2015, 2013, 2009

IEEE Transactions on Parallel and Distributed Systems (TPDS), 2013

IEEE Transactions on Very Large Scale Integration Systems (TVLSI), 2013

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2013, 2012

Journal of Computer, 2013

Journal of Software, 2013

Elsevier Journal Embedded Hardware Design (Microprocessors and Microsystems), 2013

Elsevier Journal of Parallel Computing, 2013

IEEE Transactions on Dependable and Secure Computing (TDSC), 2012

International Journal on Computer Science and Technology (JCST), 2012, 2011

ACM Journal of Emerging Technologies in Computing (ACM JETC), 2011

ACM Computing Survey (CSUR), 2011

IEEE International Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), 2011

International Journal on Software and Systems Modeling (SoSym), 2011

IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2011, 2010

IEEE Nuclear and Space Radiation Effects Conference (NSREC), 2010

IEEE International Symposium on Microarchitecture (MICRO), 2009

IEEE International Symposium on Computer Architecture and High-Performance Computing (SBAC-PAD), 2008

IEEE Conference on Nanotechnology (IEEE-NANO), 2006

IEEE International Symposium on Workload Characterization (IISWC), 2005

IEEE International Conference on Embedded Software and Systems (ICESS), 2005

- **University Service**

University of Kansas:

EECS Department Faculty Search Committee on the area of digital system design, August 2013 ~ July 2014

EECS Department Student Award Committee, August 2013~ July 2014

EECS Department Graduate Committee, August 2012 ~ July 2013

EECS Department Faculty Search Committee on the area of high-performance computing, August 2012 ~ July 2014

EECS Department Scholarship Committee, August 2010 ~ July 2012

- Member of IEEE, and ACM SIGARCH (2005 ~ Present)
- Member of Women in Computer Architecture (WICArch)

Professional Talks

- "Energy-Efficient Computing through Integration with Emerging Technologies", CS Department, Texas Southern University, February 9, 2015
- "Energy-Efficient Computing through Integration with Emerging Technologies", HP R&D Engineering Seminar Program, Houston, TX, February 5, 2015
- CF'13, "Cost-Effective Soft-Error Protection for SRAM-Based Structures in GPGPUs", Ischia, Italy, May 16, 2013
- ISQED'13, "Reliable Express Virtual Channel Based Network-on-Chip Under the Impact of Technology Scaling", Santa Clara, California, March 6, 2013
- ISQED'13, "Hybrid CMOS-TFET Register Files for Energy-Efficient GPGPUs", Santa Clara, California, March 5, 2013
- PACT'12, "RISE: Improving Streaming Processors Reliability against Soft Errors in GPGPUs", Minneapolis, Minnesota, September 21, 2012
- IISWC'11, "Analyzing Soft-Error Vulnerability on GPGPU Microarchitecture", Austin, Texas, November 8, 2011
- DSN'10, "Architecting Reliable Multi-core Network-on-Chip for Small-Scale Processing Technology", Chicago, Illinois, June 28, 2010
- HPCA'09, "Soft Error Vulnerability Aware Process Variation Mitigation", Raleigh, North Carolina, February 16, 2009
- MICRO'08, "NBTI Tolerant Microarchitecture Design in the Presence of Process Variation", Lake Como, Italy, November 12, 2008
- ICPP'08, "Optimizing Issue Queue Reliability to Soft Error on Simultaneous Multithreaded Architectures", Portland, Oregon, September 9, 2008
- DSN'08, "Combined Circuit and Microarchitecture Techniques for Effective Soft Error Robustness in SMT Processors", Anchorage, Alaska, June 26, 2008
- UCAS'08, "Optimizing Issue Queue Reliability to Soft Error on Simultaneous Multithreaded Architectures", Austin, Texas, April 20, 2008
- NSF Center for Autonomic Computing (CAC) Kickoff Meeting, "Mitigating Issue Queue Soft Error Vulnerability in Multithreaded Execution Environment", Gainesville, Florida, April 9, 2008
- NSF Center for Autonomic Computing (CAC) Planning Workshop, "Mitigating Issue Queue Soft Error Vulnerability in Multithreaded Execution Environment", Gainesville, Florida, September 6, 2007

- MASCOTS'06, "Characterizing Microarchitecture Soft Error Vulnerability Phase Behavior", Monterey, California, September 12, 2006
- MOBS'06, "Sim-SODA: A Unified Framework for Architectural Level Software Reliability Analysis", Boston, Massachusetts, June 18, 2006